



WANic™ 56512 Packet Processor

Intelligent High-Performance 10 Gigabit Ethernet Packet Processor PCI-Express Card

Interface Support

- Supports the intelligent high-performance Cavium OCTEON™ Plus 12-core 750 MHz CN5650 processor
- Up to 4 GB of high-speed DDR2 SDRAM Packet Memory via VLP Mini-RDIMMs (4 GB standard)
- Front panel access ports for 10 Gb Ethernet via two 10GBase-SR/LR SFP+ transceivers
- 32 MB of DDR SDRAM persistent memory
- Up to 4 GB USB Flash Disk (2 GB standard)
- 4 lane PCI-Express host interface

Compliance/Form Factor

- PCI-SIG – PCI-Express CEM R1.1 compliant
- PCI-SIG – PCI-Express Base R1.1 compliant
- PCI single slot card
- Designed for NEBS compliance

Software Support available

- Popular Cavium/Debian Linux® Support Package and Device Drivers
- Embedded boot loader and diagnostics (POST)

Applications

- Session Border Controller (SBC)
- Secure Access (IPsec)
- Network Address Translation (NAT)
- Traffic Management
- Firewall
- Deep Packet Inspection (DPI) and Lawful Intercept

Product Reliability

- Reliability calculated via Telcordia SR332 Issue 1
- Technical support for OEM customers and resellers

The WANic™ 56512 is an intelligent, high performance Packet Processor based on the OCTEON™ Plus multi-core processor. Ideal for IP communications networks, the WANic packet processor can be configured to enable a wide variety of applications such as demanding wire-speed communications for secure IP access.

The WANic 56512 provides a 12-core Cavium OCTEON™ Plus CN5650 processor at up to 750 MHz with 2 Mbytes (MB) of shared L2 cache memory, delivering up to 10 Gb/s line-speed packet processing for Layers 2-7. Up to 4 GBytes (GB) of high-speed DDR2 Packet Memory is implemented using VLP Mini-RDIMM modules. Thirty-two megabytes of DDR SDRAM persistent memory for storing state information is included. Up to 4 GB of Flash Disk is available for bulk memory storage.

To optimize application performance, the CN5650 supports a dual-issue, five-stage pipeline and optimized latencies as well as auto instruction pre-fetching and advanced data prefetching features to minimize memory delays.

WANic 56512 supports high-speed communications to the host via a four lane PCI-Express bus interface.

For application flexibility, the WANic 56512 supports two 10 Gb Ethernet SFP+ transceivers via the front panel, with options for SR/LR fiber or Direct Attach copper interfaces for the line connection.

Software

The WANic 56512 software implementation is a comprehensive development package designed to improve time-to-revenue. It is optimized to simplify application integration for multi-core processor development environments.

At its lowest level, the software includes a Universal Boot (U-Boot) loader and comprehensive Power On Self Test (POST) firmware embedded in the product. This boot package is loaded from Flash memory or via the host PCI-Express bus.

A Linux Support Package (LSP) and sample application code, designed to exercise the packet processor, is provided to aid in application development. This LSP includes a Linux Operating System and user application code from a TFTP server, Flash memory or via the host PCI-Express bus, and includes a well-defined Application Program Interface (API) to ease application development. Support for other operating systems is available upon request.

To further improve customer time-to-market, optional software modules such as an IPv4/IPv6 stack, IPsec, QoS management, multicast forwarding, IP filtering, VLAN, L2 tunneling and application programming frameworks are available from GE Fanuc and/or its partners.



