

New!



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- L-Band RF tuner
- Two 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multi-module synchronization
- PCI Express (Gen. 1 & 2) interface up to x8 wide
- VITA 42.0 XMC compatible with switched fabric interfaces
- User-configurable gigabit serial interface
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 71690 is a member of the Cobalt™ family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71690 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71690 factory-installed functions include two A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal

generator, and a PCIe interface complete the factory-installed functions and enable the 71690 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

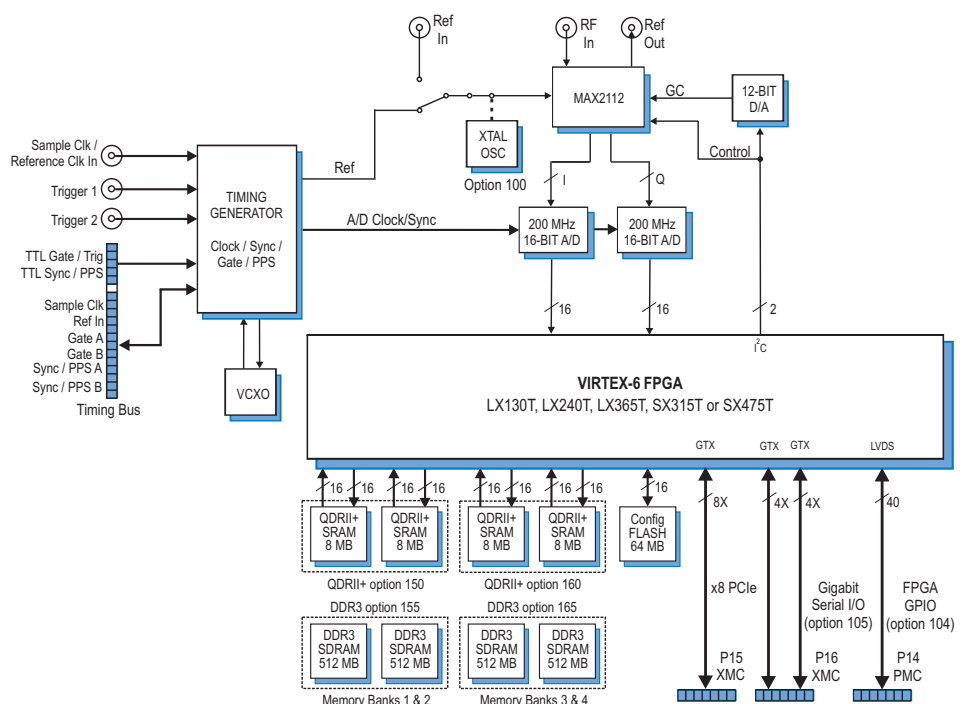
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T LX240T, LX365T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support a variety of serial protocols. ➤



### ► RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). A Maxim MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase-locked loop) synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to an on-board crystal, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable-gain range of more than 80 dB.

An integrated lowpass filter with variable bandwidth provides bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

### A/D Converter Stage

The analog baseband I and Q analog tuner outputs are then applied to two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

### A/D Clocking and Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the module. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave modules, supporting synchronous sampling and sync functions across all connected modules.

### Memory Resources

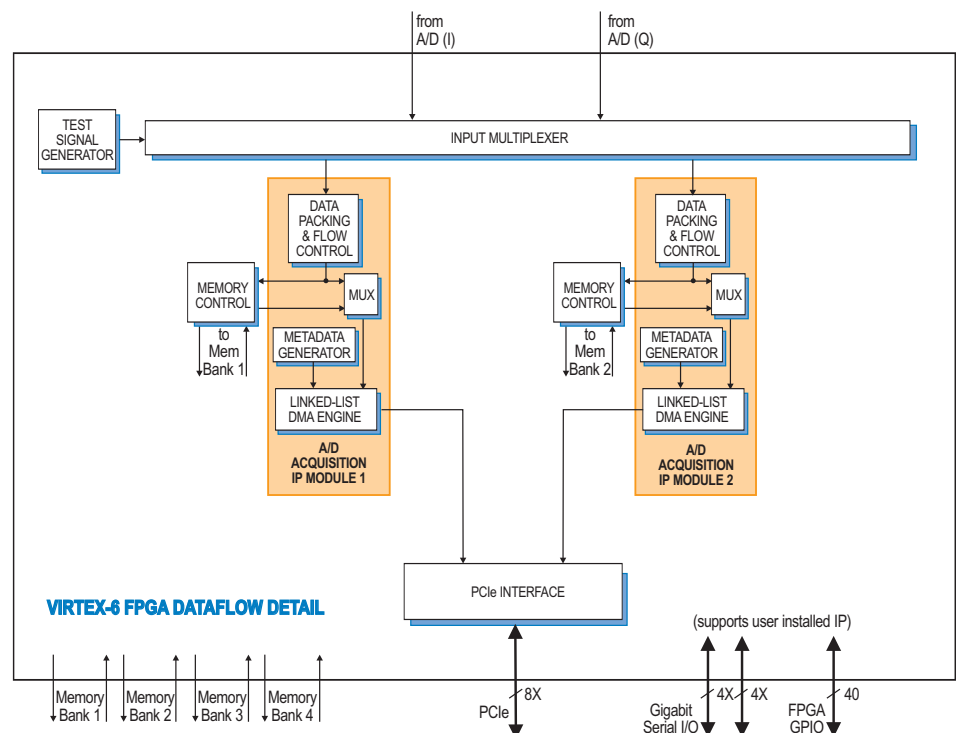
The 71690 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory. ►

### A/D Acquisition IP Modules

The 71690 features two A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.



► Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

The factory installed A/D Acquisition Modules use memory banks 1 & 2. Banks 3 & 4 can be optionally installed to support custom user-installed IP within the FPGA.

### XMC Interface

The Model 71690 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 3.125 GHz bit clock. With dual XMC connectors, the 71690 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

### PCI Express Interface

The Model 71690 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

### Specifications

#### Front Panel Analog Signal Input

**Connector:** Front panel female SSMC

**Impedance:** 50 ohms

#### L-Band Tuner

**Type:** Maxim MAX2112

**Input Frequency Range:**

925 MHz to 2175 MHz

**Monolithic VCO Phase Noise:**

-97 dBc/Hz at 10 kHz

**Fractional-N PLL Synthesizer:**

$\text{freq}_{\text{VCO}} = (N.F) \times \text{freq}_{\text{REF}}$   
where integer N = 19 to 251 and

fractional F is a 20-bit binary value

**PLL Reference ( $\text{freq}_{\text{REF}}$ ):** Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz

**LNA Gain:** 0 to 65 dB, controlled by a programmable 12-bit D/A converter

**Baseband Amplifier Gain:**

0 to 15 dB, in 1 dB steps

**Baseband Low Pass Filter:**

Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution

**Dynamic Range:** -75 dBm to 0 dBm

#### A/D Converters

**Type:** Texas Instruments ADS5485

**Sampling Rate:** 10 MHz to 200 MHz

**Resolution:** 16 bits

**Sample Clock Sources:** On-board timing generator/synthesizer

#### A/D Clock Synthesizer

**Clock Source:** Selectable from on-board programmable VCXO, front panel

external clock or LVPECL timing bus

**Synchronization:** VCXO lockable to a front panel 5 or 10 MHz reference

**VCXO Tuning Range:** 10 to 800 MHz

**A/D Clock Divider:** External clock or

VCXO can be divided by 1, 2, 4, 8, or 16

**Timing Generator External Clock Input:**

**Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

**Function:** 10 to 500 MHz A/D clock or 5 or 10 MHz VCXO PLL reference

**Timing Generator Bus:** 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

#### External Trigger Input

**Quantity:** 2

**Type:** Front panel female SSMC connector, LVITTL

**Function:** Programmable functions include: trigger, gate, sync and PPS

#### Field Programmable Gate Array

**Standard:** Xilinx Virtex-6 XC6VLX130T

**Optional:** Xilinx Virtex-6 XC6VLX240T, XC6VLX365T, XC6VSX315T, or XC6VSX475T

#### Custom I/O

**Option -104:** Installs PMC P14 connector with 20 LVDS pairs to the FPGA

**Option -105:** Installs XMC P16 connector configurable as two 4X or one 8X gigabit serial links to the FPGA

#### Memory

**Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks

**Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks

#### PCI-Express Interface

**PCI Express Bus:** Gen. 1 x8 or Gen. 2 x4

#### Environmental

**Operating Temp:** 0° to 50° C

**Storage Temp:** -20° to 90° C

**Relative Humidity:** 0 to 95%, non-cond.

**Size:** Standard XMC module, 2.91 in. x 5.87 in.

## Ordering Information

### Model Description

71690 L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - XMC

### Options:

-062 XC6VLX240T FPGA  
 -063 XC6VLX365T FPGA  
 -064 XC6VSX315T FPGA  
 -065 XC6VSX475T FPGA  
 -100 On-board 27 MHz crystal oscillator reference  
 -104 LVDS FPGA I/O through P14 connector  
 -105 Gigabit serial FPGA I/O through P16 connector  
 -150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)  
 -160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)  
 -155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)  
 -165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of conduction-cooled versions